## REMARKS

Claims 1-30 are pending in the present application. Claims 1, 4-7, 9-21, 23 and 25-29 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

Paragraph 2 of the Office Action makes reference to an Information Disclosure Statement (IDS) submitted on January 6, 2003. This reference is believed to be in error, since no IDS was submitted by the applicant on that date.

The applicant notes with appreciation that the Office Action indicates that claims 23-30 would be allowed if corrected to overcome the objections set forth in the Office Action. The claims are amended above in accordance with the suggestions made in the Office Action. No new matter is added. Entry of the amendments, removal of the objections, and allowance of claims 23-30 are respectfully requested.

The applicant notes with appreciation that the Office Action indicates that claims 4-7, 9-12, and 14-21 would be allowable if rewritten in independent form. Applicant wishes to defer submission of these claims, pending consideration of the present Amendment.

Claims 1, 4-7, and 9-29 are objected to for various informalities. The claims are amended above in a manner consistent with suggestions provided in the Office Action. Entry of the amendments and removal of the rejections are respectfully requested.

Claims 1-3, 8, 13 and 22 stand rejected under 35 U.S.C. 102(a) as being anticipated by Kim (KR Pub. No. 2002-424161). Reconsideration and removal of the rejections are respectfully requested in view of the following remarks.

The present invention of amended independent claim 1 is directed to a data output circuit. A first inversion unit receives, at an input thereof, a first data signal of an operating voltage level and inverts the received first data signal to obtain, at an output thereof, a first inverted data signal. A first voltage compensation unit coupled to the output of the first inversion unit compensates for the voltage level of the first inverted data signal to obtain a first driving signal when a first power supply voltage of an output voltage level is different from a second power supply voltage of the operating voltage by at least a predetermined voltage level. A second

inversion unit receives, at an input thereof, a second data signal with the operating voltage level and inverts the received second data signal to obtain, at an output thereof, a second inverted data signal. A second voltage compensation unit coupled to the output of the second inversion unit compensates for the voltage level of the second inverted data signal to obtain a second driving signal, when the levels of the first and second power supplies are different by at least a predetermined voltage level. A driver unit receives the first and second driving signals and outputs an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

The present invention of amended independent claim 13 is directed to a data output circuit. A first inversion unit receives, at an input thereof, a first data signal of an operating voltage level and inverts the received first data signal to obtain, at an output thereof, a first inverted data signal when an output voltage level of a first power supply voltage is equal to an operating voltage level of a second power supply voltage. A first voltage compensation unit coupled to the output of the first inversion unit compensates for the voltage level of the first inverted data signal to obtain a first driving signal when the first power supply voltage of the output voltage level is different from the second power supply voltage of the operating voltage level is different by at least a predetermined voltage level. A second inversion unit receives, at an input thereof, a second data signal of the operating voltage level and inverts the received second data signal to obtain, at an output thereof, a second inverted data signal when the levels of the first and second power supply voltages are the same. A second voltage compensation unit coupled to the output of the second inversion unit compensates for the voltage level of the second inverted data signal to obtain a second driving signal when the levels of the first and second power supply voltages are different by at least a predetermined voltage level. A driver unit receives the first and second driving signals and outputs an output data signal of a logic level that is opposite the logic levels of the first and second driving signals.

In the present invention as claimed in amended independent claims 1 and 13, a first inversion unit receives, at an input thereof, a first data signal of an operating voltage level and inverts the received first data signal to obtain, at an output thereof, a first inverted data signal. A first voltage compensation unit coupled to the output of the first inversion unit compensates for the voltage level of the first inverted data signal to obtain a first driving signal, when a first power supply voltage of an output voltage level is different from a second power supply voltage of the operating voltage level by at least a predetermined voltage level. Similarly, a second

inversion unit receives, at an input thereof, a second data signal with the operating voltage level and inverts the received second data signal to obtain, at an output thereof, a second inverted data signal. A second voltage compensation unit coupled to the output of the second inversion unit compensates for the voltage level of the second inverted data signal to obtain a second driving signal, when the levels of the first and second power supply voltages are different by at least a predetermined voltage level. This feature is illustrated at least at FIGs. 3, 5, and 7 of the present specification, which depicts a first inversion unit 330, 530, 730 receiving, at an input thereof, a first data signal DATA1 and inverting the received first data signal DATA1 to obtain, at an output thereof, a first inverted data signal /DATA1. A first voltage compensation unit 340, 540, 740 coupled to the output of the first inversion unit 330, 530, 730 compensates for the voltage level of the first inverted data signal /DATA1 to obtain a first driving signal DRV1. For example, the PMOS transistor MPC2 of the first voltage compensation unit 340, 540, 740 is coupled to the output node of the first inversion unit 330, 530, 730 at the junction between PMOS transistor MP1, MPA1 and NMOS transistor MN1, MNA1. Similarly, a second inversion unit 350, 550, 750 receives, at an input thereof, a second data signal DATA2 and inverts the received second data signal DATA2 to obtain, at an output thereof, a second inverted data signal /DATA2. A second voltage compensation unit 360, 560,760 coupled to the output of the second inversion unit 350, 550,750 compensates for the voltage level of the second inverted data signal /DATA2 to obtain a second driving signal DRV2.

The Kim reference is cited in the Office Action at page 4 as teaching a "first inversion unit" at first input stage 100, a "second inversion unit" at second input stage 102, a "first voltage compensation unit" at first voltage compensation portion 104, and a "second voltage compensation unit" at second voltage compensation portion 106. In Kim, however, the first voltage compensation portion 104 is not coupled to the output of the first input stage 100. Instead, Kim discloses the first voltage compensation portion 104 (including NMOS transistor MN22 and capacitor C10) coupled between the first input stage 100 (including PMOS transistor MP20 and NMOS transistor MN20) and ground voltage. In Kim, the output of the first input stage 100 is the node between the input stage 100 (at the junction of PMOS transistor MP20 and NMOS transistor MN20) and the gate of the PMOS transistor MP23 of the output stage 108. The control transistor MN22 of the first voltage compensation portion 140 is connected between NMOS transistor MN20 and ground, and is not coupled to the output of the first input stage 100. Thus, it is respectfully submitted that Kim fails to disclose "...a first voltage compensation unit coupled to the output of the first inversion unit...", as claimed in amended independent claims 1

and 13. For the same reasons, it is respectfully submitted that Kim further fails to disclose "...a second voltage compensation unit coupled to the output of the second inversion unit..." as claimed in independent claims 1 and 13.

It is further submitted that Kim fails to teach or suggest a "first (second) voltage compensation unit...that compensates for the voltage level of the first (second) inverted data signal to obtain a first (second) driving signal, when a first power supply voltage of an output voltage level is different from a second power supply voltage of the operating voltage level by at least a predetermined voltage level," as claimed in claims 1 and 13. Specifically, Kim makes no such determination as to whether the "output voltage level" of the first (second) power supply voltage and the "operating voltage level" of the second power supply voltage are different by a "predetermined voltage level", as claimed.

In view of the above, it is submitted that Kim fails to teach or suggest the present invention as claimed in independent claims 1 and 13. Reconsideration and removal of the rejection and allowance of the claims are therefore respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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